

REMARKS

This amendment is in response to the Advisory Action dated February 20, 2008. Claims 1, 10, 17, 40, and 54 have been amended, claims 2 and 3 have been cancelled; as such claims 1, 10-25, 40-45, 54-63 are now pending in this application. Claims 1, 10, 17, 40, and 54 are independent claims. Reconsideration and allowance is requested in view of the claim amendments and the following remarks.

Summary of Examiner Interview

Initially, Applicant wishes to thank Examiner Dharia for his time at the interview of March 4, 2008, the contents of which are summarized below. Prior to the Interview, The Examiner contacted Applicant's representative to discuss issues pertaining to the prior art rejection and the double patenting rejection.

At the Interview, The Examiner indicated that Applicant's argument could prove more persuasive if Applicant were to consider various suggested amendments, particularly emphasizing that the polarized switches are P-channel and N-channel transistors, as well as the fact that, unlike the prior art reference, the present application includes P-channel and N-channel transistors positioned adjacently, corresponding to the bits of the n-bit signal. The Examiner also suggested incorporating the subject matter of claim 3 into the independent claims along with further amendments.

After the interview, Applicant's representative provided the Examiner with potential amendments to the independent claims. Thereafter, the Examiner contacted Applicant's representative to confirm receipt and approval of the suggested claims, incorporated into this amendment.

Double Patenting Rejection

Claims 1-3, 10-25, 40-45, and 54-58 can be rejected on the ground of nonstatutory double-patenting over claims in U.S. Patent No. 6,664,943.

The current application is a child/divisional of parent/App. No. 09/466,969 (U.S. Patent No. 6,664,943) resulting from a Restriction Requirement issued on October 4, 2002 by Examiner Xiao Min Wu on the parent application. Accordingly, the present application should not qualify for a double patenting rejection.

Furthermore, the present claims may also overcome any Double Patenting Issues.

Rejection under 35 U.S.C. § 102 and 35 U.S.C. § 103

Claims 1-3 have been rejected under 35 U.S.C. § 102 as anticipated over U.S. Patent No. 6,911,926 to Koyoma et al. ("Koyoma"); Claims 10-25, 40-45, and 54-58 have been rejected under 35 U.S.C. § 103 as obvious over Koyoma in view of U.S. Patent No. 6,274,869 to Butler et al. ("Butler").

The claim amendments provided in this amendment address the Examiner's concerns discussed at the Interview of March, 4, 2008. In particular, the independent claims now provide that "*the analog switches polarized comprise P-channel MOS transistors and N-channel MOS transistors*" and that "*the n-bit digital data signal has a low amplitude equal to a reference voltage minimum less a threshold value of a P-channel MOS transistor and a high amplitude equal to a reference voltage maximum plus a threshold of an N-channel MOS transistor.*" As, such the claims are distinguishable from the transistor layout disclosed in Koyoma.

Accordingly, Applicant respectfully requests that the rejections under 35 U.S.C. § 102 and § 103 be withdrawn.

CONCLUSION

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 18-0013, under Order No. SON-1697/DIV from which the undersigned is authorized to draw.

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Respectfully submitted,

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